

Tiziana Margaria
Tom Melham (Eds.)

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Correct Hardware Design and Verification Methods

**11th IFIP WG 10.5 Advanced Research
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Livingston, Scotland, UK, September 2001, Proceedings**



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Correct Hardware Design And Verification Methods

**Ganesh Gopalakrishnan, Phillip
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Correct Hardware Design And Verification Methods:

Correct Hardware Design and Verification Methods, 1995 *Correct Hardware Design and Verification Methods* Dominique Borrione, 2005-09-19 This book constitutes the refereed proceedings of the 13th IFIP WG 10.5 Advanced Research Working Conference on Correct Hardware Design and Verification Methods CHARME 2005 held in Saarbrücken Germany in October 2005. The 21 revised full papers and 18 short papers presented together with 2 invited talks and one tutorial were carefully reviewed and selected from 79 submissions. The papers are organized in topical sections on functional approaches to design description game solving approaches abstraction algorithms and techniques for speeding DD based verification real time and LTL model checking evaluation of SAT based tools model reduction and verification of memory hierarchy mechanisms.

Correct Hardware Design and Verification Methods Daniel Geist, Enrico Tronci, 2003-10-22 This book constitutes the refereed proceedings of the 12th IFIP WG 10.5 Advanced Research Working Conference on Correct Hardware Design and Verification Methods CHARME 2003 held in L'Aquila Italy in October 2003. The 24 revised full papers and 8 short papers presented were carefully reviewed and selected from 65 submissions. The papers are organized in topical sections on software verification automata based methods processor verification specification methods theorem proving bounded model checking and model checking and applications.

Correct Hardware Design and Verification Methods Paolo Camurati, 1995-09-18 This book constitutes the refereed proceedings of the IFIP WG10.5 Advanced Research Working Conference on Correct Hardware Design Methodologies CHARME 95 held in Frankfurt Germany in October 1995. The 20 revised full papers presented were carefully selected by the program committee and address all current aspects of research and advanced applications in the field of formal verification of hardware. Among the topics covered are model checking theorem proving formally verified synthesis process algebras finite state systems verification environments language containment and VHDL.

Correct Hardware Design and Verification Methods Tiziana Margaria, Tom Melham, 2003-06-30 This volume contains the proceedings of CHARME 2001 the Eleventh Advanced Research Working Conference on Correct Hardware Design and Verification Methods. CHARME 2001 is the 11th in a series of working conferences devoted to the development and use of leading edge formal techniques and tools for the design and verification of hardware and hardware like systems. Previous events in the CHARME series were held in Bad Herrenalb 1999 Montreal 1997 Frankfurt 1995 Arles 1993 and Torino 1991. This series of meetings has been organized in cooperation with IFIP WG 10.5 and WG 10.2. Prior meetings stretching back to the earliest days of formal hardware verification were held under various names in Miami 1990 Leuven 1989 Glasgow 1988 Grenoble 1986 Edinburgh 1985 and Darmstadt 1984. The convention is now well established whereby the European CHARME conference alternates with its biennial counterpart the International Conference on Formal Methods in Computer Aided Design FMCAD which is held on even numbered years in the USA. The conference took place during 4-7 September 2001 at the Institute for System Level Integration in Livingston Scotland. It was co-hosted by

the Institute and the Department of Computing Science of Glasgow University and co sponsored by the IFIP TC10 WG10 5 Working Group on Design and Engineering of Electronic Systems CHARME 2001 also included a scientific session and social program held jointly with the 14th International Conference on Theorem Proving in Higher Order Logics TPHOLs which was co located in nearby Edinburgh

Correct Hardware Design and Verification Methods, 1995 **Correct Hardware Design and Verification Methods** Laurence Pierre, Thomas Kropf, 2003-07-31 CHARME 99 is the tenth in a series of working conferences devoted to the development and use of leading edge formal techniques and tools for the design and verification of hardware and systems Previous conferences have been held in Darmstadt 1984 Edinburgh 1985 Grenoble 1986 Glasgow 1988 Leuven 1989 Torino 1991 Arles 1993 Frankfurt 1995 and Montreal 1997 This workshop and conference series has been organized in cooperation with IFIP WG 10 5 It is now the biannual counterpart of FMCAD which takes place every even numbered year in the USA The 1999 event took place in Bad Herrenalb a resort village located in the Black Forest close to the city of Karlsruhe The validation of functional and timing behavior is a major bottleneck in current VLSI design systems A predominantly academic area of study until a few years ago formal design and verification techniques are now migrating into industrial use The aim of CHARME 99 is to bring together researchers and users from academia and industry working in this active area of research Two invited talks illustrate major current trends the presentation by Gerard Berry Ecole des Mines de Paris Sophia Antipolis France is concerned with the use of synchronous languages in circuit design and the talk given by Peter Jansen BMW Munich Germany demonstrates an application of formal methods in an industrial environment The program also includes 20 regular presentations and 12 short presentations poster exhibitions that have been selected from the 48 submitted papers

Correct Hardware Design and Verification Methods Paolo Enrico Camurati, Hans Eveking, 2014-03-12 This book constitutes the refereed proceedings of the IFIP WG10 5 Advanced Research Working Conference on Correct Hardware Design Methodologies CHARME 95 held in Frankfurt Germany in October 1995 The 20 revised full papers presented were carefully selected by the program committee and address all current aspects of research and advanced applications in the field of formal verification of hardware Among the topics covered are model checking theorem proving formally verified synthesis process algebras finite state systems verification environments language containment and VHDL

Formal Methods in Computer-Aided Design Mandayam Srivas, Albert Camilleri, 1996-10-23 This book constitutes the refereed proceedings of the First International Conference on Formal Methods in Computer Aided Design FMCAD 96 held in Palo Alto California USA in November 1996 The 25 revised full papers presented were selected from a total of 65 submissions also included are three invited survey papers and four tutorial contributions The volume covers all relevant formal aspects of work in computer aided systems design including verification synthesis and testing

Formal Methods in Computer-Aided Design Ganesh Gopalakrishnan, Phillip Windley, 2003-07-31 This book constitutes the refereed proceedings of the Second International Conference on Formal Methods in Computer Aided Design FMCAD 98

held in Palo Alto California USA in November 1998 The 27 revised full papers presented were carefully reviewed and selected from a total of 55 submissions Also included are four tools papers and four invited contributions The papers present the state of the art in formal verification methods for digital circuits and systems including processors custom VLSI circuits microcode and reactive software From the methodological point of view binary decision diagrams model checking symbolic reasoning symbolic simulation and abstraction methods are covered

Formal Logical Methods for System Security and Correctness Orna Grumberg, Tobias Nipkow, Christian Pfaller, 2008 Offers information in the field of proof technology in connection with secure and correct software This title shows that methods of correct by construction program and process synthesis allow a high level programming method more amenable to security and reliability analysis and guarantees

Model Checking, second edition Edmund M. Clarke, Jr., Orna Grumberg, Daniel Kroening, Doron Peled, Helmut Veith, 2018-12-04 An expanded and updated edition of a comprehensive presentation of the theory and practice of model checking a technology that automates the analysis of complex systems Model checking is a verification technology that provides an algorithmic means of determining whether an abstract model representing for example a hardware or software design satisfies a formal specification expressed as a temporal logic formula If the specification is not satisfied the method identifies a counterexample execution that shows the source of the problem Today many major hardware and software companies use model checking in practice for verification of VLSI circuits communication protocols software device drivers real time embedded systems and security algorithms This book offers a comprehensive presentation of the theory and practice of model checking covering the foundations of the key algorithms in depth The field of model checking has grown dramatically since the publication of the first edition in 1999 and this second edition reflects the advances in the field Reorganized expanded and updated the new edition retains the focus on the foundations of temporal logic model while offering new chapters that cover topics that did not exist in 1999 propositional satisfiability SAT based model checking counterexample guided abstraction refinement and software model checking The book serves as an introduction to the field suitable for classroom use and as an essential guide for researchers

Correct Hardware Design and Verification

Methods Daniel Geist, Enrico Tronci, 2014-03-12 *Fundamentals and Standards in Hardware Description Languages* Jean Mermet, 2012-12-06 The second half of this century will remain as the era of proliferation of electronic computers They did exist before but they were mechanical During next century they may perform other mutations to become optical or molecular or even biological Actually all these aspects are only fancy dresses put on mathematical machines This was always recognized to be true in the domain of software where machine or high level languages are more or less rigorous but immaterial variations of the universally accepted mathematical language aimed at specifying elementary operations functions algorithms and processes But even a mathematical machine needs a physical support and this is what hardware is all about The invention of hardware description languages HDL s in the early 60 s was an attempt to stay longer at an abstract level in

the design process and to push the stage of physical implementation up to the moment when no more technology independent decisions can be taken It was also an answer to the continuous exponential growth of complexity of systems to be designed This problem is common to hardware and software and may explain why the syntax of hardware description languages has followed with a reasonable delay of ten years the evolution of the programming languages at the end of the 60s they were Algol like a decade later Pascal like and now they are C or ADA like They have also integrated the new concepts of advanced software specification languages

Correct Hardware Design and Verification Methods George J. Milne, Laurence Pierre, 2014-03-12 These proceedings contain the papers presented at the Advanced Research Working Conference on Correct Hardware Design Methodologies held in Arles France in May 1993 and organized by the ESPRIT Working Group 6018 CHARME 2 and the Universit de Provence Marseille in cooperation with IFIP Working Group 10.2 Formal verification is emerging as a plausible alternative to exhaustive simulation for establishing correct digital hardware designs The validation of functional and timing behavior is a major bottleneck in current VLSI design systems slowing the arrival of products in the marketplace with its associated increase in cost From being a predominantly academic area of study until a few years ago formal design and verification techniques are now beginning to migrate into industrial use As we are now witnessing an increase in activity in this area in both academia and industry the aim of this working conference was to bring together researchers and users from both communities

Correct Hardware Design and Verification Methods : IFIP WG10.2 Advanced Research Working Conference, CHARME '93, Arles, France, May 24-26, 1993 : Proceedings CHARME '93, 1993 These proceedings contain the papers presented at the Advanced Research Working Conference on Correct Hardware Design Methodologies held in Arles France in May 1993 and organized by the ESPRIT Working Group 6018 CHARME 2 and the Universit de Provence Marseille in cooperation with IFIP Working Group 10.2 Formal verification is emerging as a plausible alternative to exhaustive simulation for establishing correct digital hardware designs The validation of functional and timing behavior is a major bottleneck in current VLSI design systems slowing the arrival of products in the marketplace with its associated increase in cost From being a predominantly academic area of study until a few years ago formal design and verification techniques are now beginning to migrate into industrial use As we are now witnessing an increase in activity in this area in both academia and industry the aim of this working conference was to bring together researchers and users from both communities

Correct Hardware Design Methodologies Paolo Prinetti, Paolo Camurati, 1992 The increasing interest in formal verification of hardware is witnessed by academic and industrial research efforts multinational research projects and conferences These proceedings contain the papers presented at the Workshop held in Turin Italy from 12-14 June 1991 Papers focus on the practical impact of formal techniques in VLSI design and verification semantics for hardware description languages proof environments and methodologies Preliminary results of the ESPRIT Basic Research Action 3216 CHARME are discussed Finite State Machines and their verification semantics for

hardware description languages proof environments and methodologies as well as examples of verified circuits and Design for Verifiability are also presented

Correct Hardware Design and Verification Methods George J. Milne, Laurence Pierre, 1993-05-12 These proceedings contain the papers presented at the Advanced Research Working Conference on Correct Hardware Design Methodologies held in Arles France in May 1993 and organized by the ESPRIT Working Group 6018 CHARME 2 and the Universit de Provence Marseille in cooperation with IFIP Working Group 10 2 Formal verification is emerging as a plausible alternative to exhaustive simulation for establishing correct digital hardware designs The validation of functional and timing behavior is a major bottleneck in current VLSI design systems slowing the arrival of products in the marketplace with its associated increase in cost From being a predominantly academic area of study until a few years ago formal design and verification techniques are now beginning to migrate into industrial use As we are now witnessing an increase in activity in this area in both academia and industry the aim of this working conference was to bring together researchers and users from both communities

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