

Defect and Fault Tolerance in VLSI Systems

Volume 2

Edited by
C. H. Stapper, V. K. Jain,
and G. Saucier

Defect And Fault Tolerance In Vlsi Systems

Israel Koren



Defect And Fault Tolerance In Vlsi Systems:

Defect and Fault Tolerance in VLSI Systems Israel Koren, 2012-12-06 This book contains an edited selection of papers presented at the International Workshop on Defect and Fault Tolerance in VLSI Systems held October 6-7 1988 in Springfield Massachusetts Our thanks go to all the contributors and especially the members of the program committee for the difficult and time consuming work involved in selecting the papers that were presented in the workshop and reviewing the papers included in this book Thanks are also due to the IEEE Computer Society in particular the Technical Committee on Fault Tolerant Computing and the Technical Committee on VLSI and the University of Massachusetts at Amherst for sponsoring the workshop and to the National Science Foundation for supporting under grant number MIP 8803418 the keynote address and the distribution of this book to all workshop attendees The objective of the workshop was to bring together researchers and practitioners from both industry and academia in the field of defect tolerance and yield enhancement in VLSI to discuss their mutual interests in defect tolerant architectures and models for integrated circuit defects faults and yield Progress in this area was slowed down by the proprietary nature of yield related data and by the lack of appropriate forums for disseminating such information The goal of this workshop was therefore to provide a forum for a dialogue and exchange of views A follow up workshop in October 1989 with C H Stapper from IBM and V K Jain from the University of South Florida as general co chairmen is being organized

Defect and Fault Tolerance in VLSI Systems C.H. Stapper, V.K. Jain, Gabriele Saucier, 2013-06-29 Higher circuit densities increasingly more complex application objectives and advanced packaging technologies have substantially increased the need to incorporate defect tolerance and fault tolerance in the design of VLSI and WSI systems The goals of defect tolerance and fault tolerance are yield enhancement and improved reliability The emphasis on this area has resulted in a new field of interdisciplinary scientific research In fact advanced methods of defect fault control and tolerance are resulting in enhanced manufacturability and productivity of integrated circuit chips VLSI systems and wafer scale integrated circuits In 1987 Dr W Moore organized an International Workshop on Designing for Yield at Oxford University Edited papers of that workshop were published in reference II The participants in that workshop agreed that meetings of this type should be continued preferably on a yearly basis It was Dr I Koren who organized the IEEE International Workshop on Defect and Fault Tolerance in VLSI Systems in Springfield Massachusetts the next year Selected papers from that workshop were published as the first volume of this series 21

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art industrial data necessary ingredients for significant advances in this field All aspects of design manufacturing test reliability and availability that are affected by defects during manufacturing and by faults during system operation are of interest

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Defect and Fault Tolerance in VLSI Systems, 1998

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