

Defect and Fault Tolerance in VLSI Systems

Volume 2

Edited by
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and G. Saucier

Defect And Fault Tolerance In Vlsi Systems 2001

Patrick Vollmar



Defect And Fault Tolerance In Vlsi Systems 2001:

2001 IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems ,2001 This volume features the proceedings of the International Symposium on Defect and Fault Tolerance in VLSI Systems DFT 2001 Defect and Fault Tolerance in VLSI Systems Israel Koren,2012-12-06 This book contains an edited selection of papers presented at the International Workshop on Defect and Fault Tolerance in VLSI Systems held October 6 7 1988 in Springfield Massachusetts Our thanks go to all the contributors and especially the members of the program committee for the difficult and time consuming work involved in selecting the papers that were presented in the workshop and reviewing the papers included in this book Thanks are also due to the IEEE Computer Society in particular the Technical Committee on Fault Tolerant Computing and the Technical Committee on VLSI and the University of Massachusetts at Amherst for sponsoring the workshop and to the National Science Foundation for supporting under grant number MIP 8803418 the keynote address and the distribution of this book to all workshop attendees The objective of the workshop was to bring together researchers and practitioners from both industry and academia in the field of defect tolerance and yield enhancement in VLSI to discuss their mutual interests in defect tolerant architectures and models for integrated circuit defects faults and yield Progress in this area was slowed down by the proprietary nature of yield related data and by the lack of appropriate forums for disseminating such information The goal of this workshop was therefore to provide a forum for a dialogue and exchange of views A follow up workshop in October 1989 with C H Stapper from IBM and V K Jain from the University of South Florida as general co chairmen is being organized **Proceedings** ,2005 *Defect and Fault Tolerance in VLSI Systems* ,1988

Soft Errors in Modern Electronic Systems Michael Nicolaidis,2010-09-24 This book provides a comprehensive presentation of the most advanced research results and technological developments enabling understanding qualifying and mitigating the soft errors effect in advanced electronics including the fundamental physical mechanisms of radiation induced soft errors the various steps that lead to a system failure the modelling and simulation of soft error at various levels including physical electrical netlist event driven RTL and system level modelling and simulation hardware fault injection accelerated radiation testing and natural environment testing soft error oriented test structures process level device level cell level circuit level architectural level software level and system level soft error mitigation techniques The book contains a comprehensive presentation of most recent advances on understanding qualifying and mitigating the soft error effect in advanced electronic systems presented by academia and industry experts in reliability fault tolerance EDA processor SoC and system design and in particular experts from industries that have faced the soft error impact in terms of product reliability and related business issues and were in the forefront of the countermeasures taken by these companies at multiple levels in order to mitigate the soft error effects at a cost acceptable for commercial products In a fast moving field where the impact on ground level electronics is very recent and its severity is steadily increasing at each new process node impacting one after

another various industry sectors as an example the Automotive Electronics Council comes to publish qualification requirements on soft errors research and technology developments and industrial practices have evolve very fast outdated the most recent books edited at 2004

Defect and Fault Tolerance in Vlsi Systems (dft 2002), 17th Ieee International Symposium Ieee International Symposium On Defect And Fault Tolerance In Vlsi Systems,2002 2001 *International Workshop on System-Level Interconnect Prediction* ,2001 The SLIP workshop is a forum for the exchange of ideas at the interface between interconnect technology and physical design This year in recognition of the highly diverse backgrounds and motivations of the attendees SLIP 2001 has been organized around three mini tutorials a review of wire distribution models a look under the hood of a variety of system level interconnect modeling programs and back end of line yield modeling These tutorials set the scene for the paper sessions that follow Forward

Dependable Systems and Networks (DSN 2001) (Formerly FTCS) IEEE Computer Society,IEEE,PR&&&&,2001 Proceedings of a July 2001 conference covering all aspects of dependability in classical and networked computer systems as well as topical areas in IT There is a special focus on safety and security issues in embedded multimedia and Internet applications Papers are in sections on modeling algorithms software demos replication software robustness survivability and security wireless and mobile communications real time testing and runtime error detection models for fault tolerance hardware architecture and design group oriented systems and practical experiences Specific topics include model based synthesis of fault trees from MATLAB a dynamic replica selection algorithm for tolerating timing faults constructing self testable software components and intrusion tolerant group management in enclaves This volume lacks a subject index c Book News Inc

Design and Test Technology for Dependable Systems-on-Chip Ubar, Raimund,Raik, Jaan,Vierhaus, Heinrich Theodor,2010-12-31 This book covers aspects of system design and efficient modelling and also introduces various fault models and fault mechanisms associated with digital circuits integrated into System on Chip SoC Multi Processor System on Chip MPSoC or Network on Chip NoC

Defect and Fault Tolerance in VLSI Systems C.H. Stapper,V.K. Jain,Gabriele Saucier,2013-06-29 Higher circuit densities increasingly more complex application objectives and advanced packaging technologies have suhstantially increased the need to incorporate defect tolerance and fault tolerance in the design of VLSI and WSI systems The goals of defect tolerance and fault tolerance are yield enhancement and improved reliability The emphasis on this area has resulted in a new field of interdisciplinary scientific research I n fact advanced methods of defect fault control and tolerance are resulting in enhanced manufacturability and productivity of integrated circuit chips VI SI systems and wafer scale integrated circuits In 1987 Dr W Moore organized an International Workshop on Designing for Yield at Oxford University Edited papers of that workshop were published in reference II The participants in that workshop agreed that meetings of this type should he con tinued preferahly on a yearly hasis It was Dr I Koren who organized the IEEE Inter national Workshop on Defect and Fault Tolerance in VLSI Systems in Springfield Massachusetts the next year Selected papers from that workshop were

published as the first volume of this series 21 *SOC (System-on-a-Chip) Testing for Plug and Play Test Automation*
Krishnendu Chakrabarty, 2013-04-17 System on a Chip SOC integrated circuits composed of embedded cores are now commonplace Nevertheless there remain several roadblocks to rapid and efficient system integration Test development is seen as a major bottleneck in SOC design and manufacturing capabilities Testing SOCs is especially challenging in the absence of standardized test structures test automation tools and test protocols In addition long interconnects high density and high speed designs lead to new types of faults involving crosstalk and signal integrity SOC System on a Chip Testing for Plug and Play Test Automation is an edited work containing thirteen contributions that address various aspects of SOC testing SOC System on a Chip Testing for Plug and Play Test Automation is a valuable reference for researchers and students interested in various aspects of SOC testing **Defect and Fault Tolerance in VLSI Systems, IEEE International Symposium on , EH-2001** Didier Keymeulen, 2001 These proceedings contain 32 papers from the July 2001 conference in Long Beach the abstract of one invited talk is also included The focus of this year s workshop was to provide a roadmap from the current proof of concept stage of Evolvable Hardware to the development of larger scale real world systems addressing issues such as evolvability and scalability from the Preface Papers concentrate on topics like the relationships between biology and robotics the evolution of analog and mixed signal circuits survivable and flexible hardware the evolution of digital functions the evolution of signal processing circuits reconfiguration architecture and devices the evolution of CA brain inspired architecture evolvability and applications Author index only c Book News Inc Programmable Devices and Systems 2001 W. Ciazynski, W. Ciężysnki, Edward Hryniewicz, P. Kłosowski, 2002 Scientific meetings on programmable devices and systems began in 1995 with the PDS 95 event organised by the Institute of Electronics Silesian University of Technology SUT Many papers on the issues of programmable devices and systems were presented at numerous conferences and workshops devoted to electronics and circuit theory yet there were no workshops devoted solely to those particular topics Combined with the belief that some specific common problems appeared in the area of PDS justified the decision to organise the PDS meeting The PDS2001 IFAC Workshop organised by the Institute of Electronics SUT Gliwice Poland was the 5th event in the series The aim of the meeting was to define the future trends of this field via the interaction of industry technical research centres and academia representatives This Proceedings volume contains 54 duly presented papers and many of them when compared to the Preprints volume version have been corrected and enriched with the discussion results The papers are grouped according to the Workshop plenary sessions topics as follows bull Communication bull Digital Signal Processing bull Industrial Programmable Logic Controllers bull Field Programmable Logic **18th International Conference on VLSI Design** International Conference on VLSI Design, 2005 Adaptable Embedded Systems Antonio Carlos Schneider Beck, Carlos Arthur Lang Lisbôa, Luigi Carro, 2012-11-27 As embedded systems become more complex designers face a number of challenges at different levels they need to boost performance while keeping energy consumption

as low as possible they need to reuse existent software code and at the same time they need to take advantage of the extra logic available in the chip represented by multiple processors working together This book describes several strategies to achieve such different and interrelated goals by the use of adaptability Coverage includes reconfigurable systems dynamic optimization techniques such as binary translation and trace reuse new memory architectures including homogeneous and heterogeneous multiprocessor systems communication issues and NOCs fault tolerance against fabrication defects and soft errors and finally how one can combine several of these techniques together to achieve higher levels of performance and adaptability The discussion also includes how to employ specialized software to improve this new adaptive system and how this new kind of software must be designed and programmed

19th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems ,2004-01-01 DFT 2004 showcases the latest research results in the in the field of defect and fault tolerance in VLSI systems Its papers cover yield defect and fault tolerance error correction and circuit system reliability and dependability

VLSI Circuits and Systems ,2005 *Directory of Published Proceedings* ,2002 Defect and Fault Tolerance in VLSI Systems ,1998

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