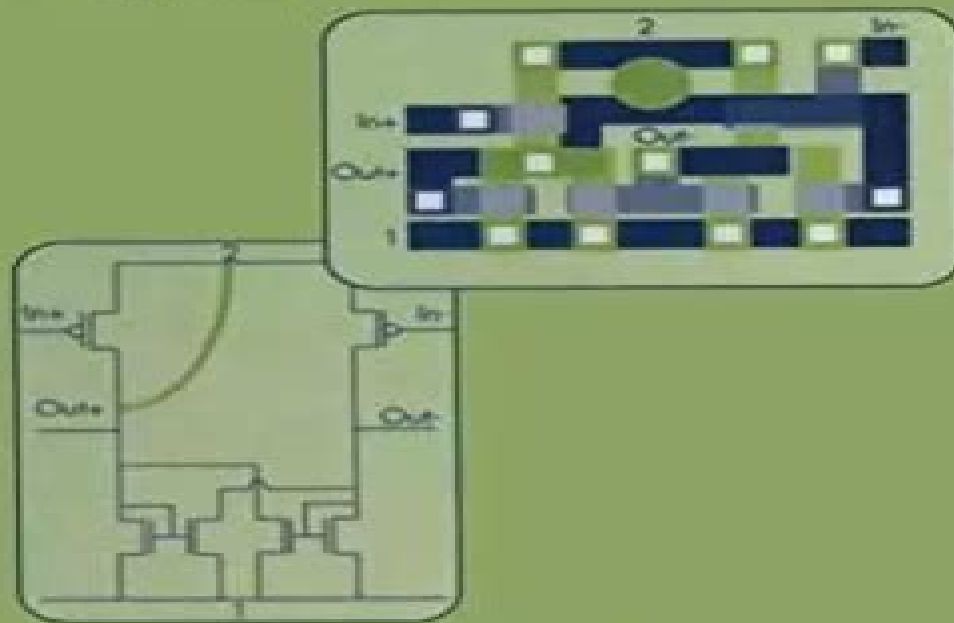


# Defect Oriented Testing for CMOS Analog and Digital Circuits

Manoj Sachdev



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# Defect Oriented Testing For Cmos Analog And Digital Circuits

**Yichuang Sun**



## **Defect Oriented Testing For Cmos Analog And Digital Circuits:**

**Defect Oriented Testing for CMOS Analog and Digital Circuits** Manoj Sachdev, 2013-06-29 Defect oriented testing is expected to play a significant role in coming generations of technology. Smaller feature sizes and larger die sizes will make ICs more sensitive to defects that can not be modeled by traditional fault modeling approaches. Furthermore, with increased level of integration, an IC may contain diverse building blocks. Such blocks include digital logic, PLAs, volatile and non-volatile memories, and analog interfaces. For such diverse building blocks, traditional fault modeling and test approaches will become increasingly inadequate. Defect oriented testing methods have come a long way from a mere interesting academic exercise to a hard industrial reality. Many factors have contributed to its industrial acceptance. Traditional approaches of testing modern integrated circuits (ICs) have been found to be inadequate in terms of quality and economics of test. In a globally competitive semiconductor market place, overall product quality and economics have become very important objectives. In addition, electronic systems are becoming increasingly complex and demand components of highest possible quality. Testing, in general, and defect oriented testing, in particular, help in realizing these objectives. **Defect Oriented Testing for CMOS Analog and Digital Circuits** is the first book to provide a complete overview of the subject. It is essential reading for all design and test professionals as well as researchers and students working in the field. A strength of this book is its breadth. Types of designs considered include analog and digital circuits, programmable logic arrays, and memories. Having a fault model does not automatically provide a test. Sometimes design for testability hardware is necessary. Many design for testability ideas supported by experimental evidence are included from the Foreword by Vishwani D. Agrawal. **Test and Diagnosis of Analogue, Mixed-signal and RF Integrated Circuits** Yichuang Sun, 2008-05-30 This book provides a comprehensive discussion of automatic testing, diagnosis, and tuning of analogue, mixed signal, and RF integrated circuits and systems in a single source. As well as fundamental concepts and techniques, the book reports systematically the state of the arts and future research directions of those areas. A complete range of circuit components are covered and test issues from the SoC perspective. An essential reference for researchers and engineers in mixed signal testing, postgraduate and senior undergraduate students. **Test and Design-for-Testability in Mixed-Signal Integrated Circuits** Jose Luis Huertas Díaz, 2010-02-23 **Test and Design for Testability in Mixed Signal Integrated Circuits** deals with test and design for test of analog and mixed signal integrated circuits. Especially in System on Chip (SoC) where different technologies are intertwined, analog, digital, sensors, RF test is becoming a true bottleneck of present and future IC projects. Linking design and test in these heterogeneous systems will have a tremendous impact in terms of test time, cost, and proficiency. Although it is recognized as a key issue for developing complex ICs, there is still a lack of structured references presenting the major topics in this area. The aim of this book is to present basic concepts and new ideas in a manner understandable for both professionals and students. Since this is an active research field, a comprehensive state of the art overview is very valuable, introducing the main

problems as well as the ways of solution that seem promising emphasizing their basis strengths and weaknesses In essence several topics are presented in detail First of all techniques for the efficient use of DSP based test and CAD test tools Standardization is another topic considered in the book with focus on the IEEE 1149 4 Also addressed in depth is the connecting design and test by means of using high level behavioural description techniques specific examples are given Another issue is related to test techniques for well defined classes of integrated blocks like data converters and phase locked loops Besides these specification driven testing techniques fault driven approaches are described as they offer potential solutions which are more similar to digital test methods Finally in Design for Testability and Built In Self Test two other concepts that were taken from digital design are introduced in an analog context and illustrated for the case of integrated filters In summary the purpose of this book is to provide a glimpse on recent research results in the area of testing mixed signal integrated circuits specifically in the topics mentioned above Much of the work reported herein has been performed within cooperative European Research Projects in which the authors of the different chapters have actively collaborated It is a representative snapshot of the current state of the art in this emergent field

Computer-Aided Design of Analog Integrated Circuits and Systems Rob A. Rutenbar, Georges G. E. Gielen, 2002-05-06 The tools and techniques you need to break the analog design bottleneck Ten years ago analog seemed to be a dead end technology Today System on Chip SoC designs are increasingly mixed signal designs With the advent of application specific integrated circuits ASIC technologies that can integrate both analog and digital functions on a single chip analog has become more crucial than ever to the design process Today designers are moving beyond hand crafted one transistor at a time methods They are using new circuit and physical synthesis tools to design practical analog circuits new modeling and analysis tools to allow rapid exploration of system level alternatives and new simulation tools to provide accurate answers for analog circuit behaviors and interactions that were considered impossible to handle only a few years ago To give circuit designers and CAD professionals a better understanding of the history and the current state of the art in the field this volume collects in one place the essential set of analog CAD papers that form the foundation of today s new analog design automation tools Areas covered are Analog synthesis Symbolic analysis Analog layout Analog modeling and analysis Specialized analog simulation Circuit centering and yield optimization Circuit testing Computer Aided Design of Analog Integrated Circuits and Systems is the cutting edge reference that will be an invaluable resource for every semiconductor circuit designer and CAD professional who hopes to break the analog design bottleneck

*Integrated Circuit Test Engineering* Ian A. Grout, 2005-12-08 Taking a three pronged approach test engineering from traditional test design and manufacturing view points Integrated Circuit Test Engineering encapsulates the subject as it stands today After introductory background from basic testing rules to trends in technology the reader learns about fabrication processes a complete range of detailed tests and procedures how to design for testability fault simulation automatic test equipment and the economics of testing The text includes Worked examples and exercises well

organized references and bibliography An introduction to the use of various software and languages such as MATLAB Spice Verilog HDL and VHDL A series of experiments based on material downloaded from springeronline com showing how to construct a hardware test arrangement for MS Windows PCs This book is a practical tool for advanced undergraduate and graduate electronic engineering students a resource for their tutors and a guide for the practising electronic engineer

*Defect-Oriented Testing for Nano-Metric CMOS VLSI Circuits* Manoj Sachdev, José Pineda de Gyvez, 2007-06-04 Defect oriented testing methods have come a long way from a mere interesting academic exercise to a hard industrial reality Many factors have contributed to its industrial acceptance Traditional approaches of testing modern integrated circuits have been found to be inadequate in terms of quality and economics of test In a globally competitive semiconductor market place overall product quality and economics have become very important objectives In addition electronic systems are becoming increasingly complex and demand components of the highest possible quality Testing in general and defect oriented testing in particular help in realizing these objectives For contemporary System on Chip SoC VLSI circuits testing is an activity associated with every level of integration However special emphasis is placed for wafer level test and final test Wafer level test consists primarily of dc or slow speed tests with current voltage checks per pin under most operating conditions and with test limits properly adjusted Basic digital tests are applied and in some cases low frequency tests to ensure analog RF functionality are exercised as well Final test consists of checking device functionality by exercising RF tests and by applying a comprehensive suite of digital test methods such as I delay fault testing DDQ stuck at testing low voltage testing etc This partitioning choice is actually application dependent

**Analog and Mixed-signal Test** Bapiraju Vinnakota, 1998 More and more chips are being designed with both analog and digital circuitry next to each other which makes testing analog circuitry even more challenging This comprehensive guide reviews all the potential testing options helping designers engineers CAD developers and researchers choose the most cost effective accurate solutions for both mixed signal and analog only testing

Proceedings , 2005      **The Cumulative Book Index** , 1999      **Defect-Oriented Testing for Nano-Metric CMOS VLSI Circuits** Manoj Sachdev, Jose Pineda de Gyvez, 2008-11-01 The 2nd edition of defect oriented testing has been extensively updated New chapters on Functional Parametric Defect Models and Inductive fault Analysis and Yield Engineering have been added to provide a link between defect sources and yield The chapter on RAM testing has been updated with focus on parametric and SRAM stability testing Similarly newer material has been incorporated in digital fault modeling and analog testing chapters The strength of Defect Oriented Testing for nano Metric CMOS VLSIs lies in its industrial relevance

*18th IEEE VLSI Test Symposium* , 2000 Proceedings of a spring 2000 symposium highlighting novel ideas and approaches to current and future problems related to testing of electronic circuits and systems Themes are microprocessor test validation low power BIST and scan technology trends scan related approaches defect driven techniques and system on chip test techniques Other subjects are analog test techniques temperature and process drift issues test

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