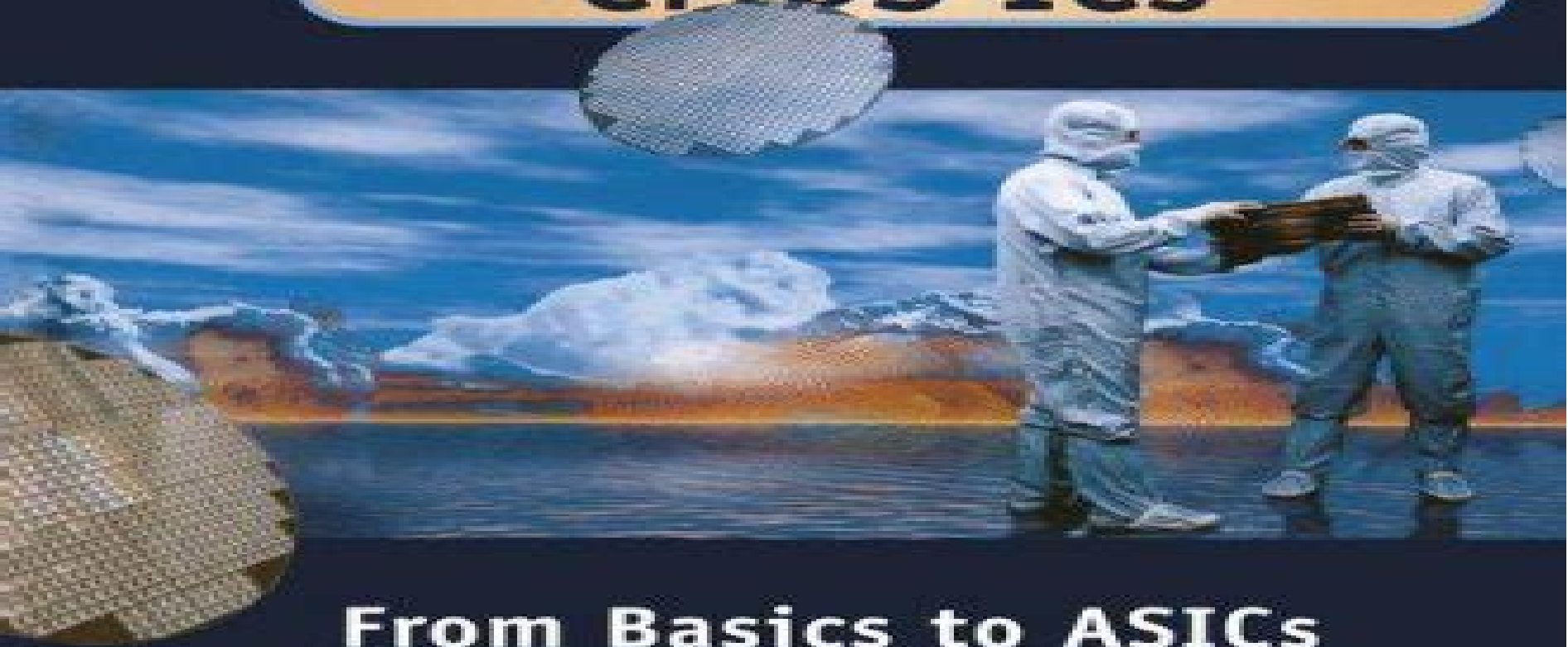


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Technology Rainer Waser, 2012-05-29 This outstanding textbook provides an introduction to electronic materials and device concepts for the major areas of current and future information technology On about 1 000 pages it collects the fundamental concepts and key technologies related to advanced electronic materials and devices The obvious strength of the book is its encyclopedic character providing adequate background material instead of just reviewing current trends It focuses on the underlying principles which are illustrated by contemporary examples The third edition now holds 47 chapters grouped into eight sections The first two sections are devoted to principles materials processing and characterization methods Following sections hold contributions to relevant materials and various devices computational concepts storage systems data transmission imaging systems and displays Each subject area is opened by a tutorial introduction written by the editor and giving a rich list of references The following chapters provide a concise yet in depth description in a given topic Primarily aimed at graduate students of physics electrical engineering and information technology as well as material science this book is equally of interest to professionals looking for a broader overview Experts might appreciate the book for having quick access to principles as well as a source for getting insight into related fields

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Christian Piguet, 2018-10-03 The power consumption of integrated circuits is one of the most problematic considerations affecting the design of high performance chips and portable devices The study of power saving design methodologies now must also include subjects such as systems on chips embedded software and the future of microelectronics Low Power Electronics Design covers all major aspects of low power design of ICs in deep submicron technologies and addresses emerging topics related to future design This volume explores in individual chapters written by expert authors the many low power techniques born during the past decade It also discusses the many different domains and disciplines that impact power consumption including processors complex circuits software CAD tools and energy sources and management The authors delve into what many specialists predict about the future by presenting techniques that are promising but are not yet reality They investigate nanotechnologies optical circuits ad hoc networks e textiles as well as human powered sources of energy Low Power Electronics Design delivers a complete picture of today's methods for reducing power and also illustrates the advances in chip design that may be commonplace 10 or 15 years from now

SOC (System-on-a-Chip) Testing for Plug and

Play Test Automation Krishnendu Chakrabarty, 2013-04-17 System on a Chip SOC integrated circuits composed of embedded cores are now commonplace Nevertheless there remain several roadblocks to rapid and efficient system integration Test development is seen as a major bottleneck in SOC design and manufacturing capabilities Testing SOCs is especially challenging in the absence of standardized test structures test automation tools and test protocols In addition long interconnects high density and high speed designs lead to new types of faults involving crosstalk and signal integrity SOC System on a Chip Testing for Plug and Play Test Automation is an edited work containing thirteen contributions that address various aspects of SOC testing SOC System on a Chip Testing for Plug and Play Test Automation is a valuable reference for researchers and students interested in various aspects of SOC testing **Low Power Interconnect Design** Sandeep Saini, 2015-06-12 This book provides practical solutions for delay and power reduction for on chip interconnects and buses It provides an in depth description of the problem of signal delay and extra power consumption possible solutions for delay and glitch removal while considering the power reduction of the total system Coverage focuses on use of the Schmitt Trigger as an alternative approach to buffer insertion for delay and power reduction in VLSI interconnects In the last section of the book various bus coding techniques are discussed to minimize delay and power in address and data buses **Frontiers In Electronics** Sorin Cristoloveanu, Michael S Shur, 2009-08-06 Frontiers in Electronics contains the selected best papers presented at the Workshop on Frontiers in Electronics WOFE 07 This meeting was the fifth in the series of WOFE workshops and strongly reinforced the tradition of scientific quality and visionary research The issues addressed ranged from THz and infrared electronics to nanoelectronics and photonics The papers focused on the fabrication characterization and applications of nanodevices wide band gap structures and state of the art FETs The participants also discussed the device physics and processing issues including aspects related to SOI and germanium on insulator technologies TFTs and advanced CMOS and MOSFETs It is this cross pollination between different but related fields that made this conference very special This book which goes beyond the publication of the WOFE Proceedings includes full length invited papers selected at the conference and reviewed by international leaders The book is divided into four distinct sections with the common denominator throughout being the nano device present under various metamorphoses in the wide CMOS and optoelectronics arena a

19th IEEE VLSI Test Symposium , 2001 Collects 58 papers from the April May 2001 symposium that explore new approaches in the testing of electronic circuits and systems Key areas in testing are discussed such as BIST analog measurement fault tolerance diagnosis methods scan chain design memory test and diagnosis and test data compression and compaction Also on the program are sessions on emerging areas that are gaining prominence including low power testing testing high speed circuits on low cost testers processor based self test techniques and core based system on chip testing Some of the topics are robust and low cost BIST architectures for sequential fault testing in datapath multipliers a method for measuring the cycle to cycle period jitter of high frequency clock signals fault equivalence identification using

redundancy information and static and dynamic extraction and test scheduling for minimal energy consumption under power constraints No subject index c Book News Inc **ISCAS 2001** ,2001 *IEEE VLSI Test Symposium* ,2001 *Defect and Fault Tolerance in VLSI Systems* Robert Aitken,2004 DFT 2004 showcases the latest research results in the in the field of defect and fault tolerance in VLSI systems Its papers cover yield defect and fault tolerance error correction and circuit system reliability and dependability *American Book Publishing Record* ,2001 *18th International Conference on VLSI Design* International Conference on VLSI Design,2005 **The British National Bibliography** Arthur James Wells,2001

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