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# Continuous-Time Sigma-Delta A/D Conversion

Fundamentals,  
Performance Limits  
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Implementations



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# Continuoustime Sigmadelta Ad Conversion Fundamentals Performance Limits And Robust Implementations

**Robert H.M. van Veldhoven, Arthur  
H.M. van Roermund**



## **Continuoustime Sigmadelta Ad Conversion Fundamentals Performance Limits And Robust Implementations:**

**Continuous-Time Sigma-Delta A/D Conversion** Friedel Gerfers, Maurits Ortmanns, 2006-02-27 Sigma delta A D converters are a key building block in wireless and multimedia applications This comprehensive book deals with all relevant aspects arising during the analysis design and simulation of the now widespread continuous time implementations of sigma delta modulators The results of several years of research by the authors in the field of CT sigma delta modulators are covered including the analysis and modeling of different CT modulator architectures CT DT loop filter synthesis a detailed error analysis of all components and possible compensation correction schemes for the non ideal behavior in CT sigma delta modulators Guidance for obtaining low power consumption and several practical implementations are also presented It is shown that all the proposed new theories architectures and possible correction techniques have been confirmed by measurements on discrete or integrated circuits Quantitative results are also provided thus enabling prediction of the resulting accuracy

**Sigma-Delta Converters: Practical Design Guide** Jose M. de la Rosa, 2018-11-05 Thoroughly revised and expanded to help readers systematically increase their knowledge and insight about Sigma Delta Modulators Sigma Delta Modulators SDMs have become one of the best choices for the implementation of analog digital interfaces of electronic systems integrated in CMOS technologies Compared to other kinds of Analog to Digital Converters ADCs Ms cover one of the widest conversion regions of the resolution versus bandwidth plane being the most efficient solution to digitize signals in an increasingly number of applications which span from high resolution low bandwidth digital audio sensor interfaces and instrumentation to ultra low power biomedical systems and medium resolution broadband wireless communications Following the spirit of its first edition Sigma Delta Converters Practical Design Guide 2nd Edition takes a comprehensive look at SDMs their diverse types of architectures circuit techniques analysis synthesis methods and CAD tools as well as their practical design considerations It compiles and updates the current research reported on the topic and explains the multiple trade offs involved in the whole design flow of Sigma Delta Modulators from specifications to chip implementation and characterization The book follows a top down approach in order to provide readers with the necessary understanding about recent advances trends and challenges in state of the art Ms It makes more emphasis on two key points which were not treated so deeply in the first edition It includes a more detailed explanation of Ms implemented using Continuous Time CT circuits going from system level synthesis to practical circuit limitations It provides more practical case studies and applications as well as a deeper description of the synthesis methodologies and CAD tools employed in the design of converters Sigma Delta Converters Practical Design Guide 2nd Edition serves as an excellent textbook for undergraduate and graduate students in electrical engineering as well as design engineers working on SD data converters who are looking for a uniform and self contained reference in this hot topic With this goal in mind and based on the feedback received from readers the contents have been revised and structured to make this new edition a unique monograph written in a didactical

pedagogical and intuitive style      *High Speed and Wide Bandwidth Delta-Sigma ADCs* Muhammed Bolatkale, Lucien J. Breems, Kofi A. A. Makinwa, 2014-05-27 This book describes techniques for realizing wide bandwidth 125MHz over sampled analog to digital converters ADCs in nano meter CMOS processes The authors offer a clear and complete picture of system level challenges and practical design solutions in high speed Delta Sigma modulators Readers will be enabled to implement ADCs as continuous time delta sigma CT modulators offering simple resistive inputs which do not require the use of power hungry input buffers as well as offering inherent anti aliasing which simplifies system integration The authors focus on the design of high speed and wide bandwidth Ms that make a step in bandwidth range which was previously only possible with Nyquist converters More specifically this book describes the stability power efficiency and linearity limits of Ms aiming at a GHz sampling frequency      CMOS Sigma-Delta Converters Jose M. de la Rosa, Rocio del Rio, 2013-03-13 A comprehensive overview of Sigma Delta Analog to Digital Converters ADCs and a practical guide to their design in nano scale CMOS for optimal performance This book presents a systematic and comprehensive compilation of sigma delta converter operating principles the new advances in architectures and circuits design methodologies and practical considerations going from system level specifications to silicon integration packaging and measurements with emphasis on nanometer CMOS implementation The book emphasizes practical design issues from high level behavioural modelling in MATLAB SIMULINK to circuit level implementation in Cadence Design FrameWork II As well as being a comprehensive reference to the theory the book is also unique in that it gives special importance on practical issues giving a detailed description of the different steps that constitute the whole design flow of sigma delta ADCs The book begins with an introductory survey of sigma delta modulators their fundamentals architectures and synthesis methods covered in Chapter 1 In Chapter 2 the effect of main circuit error mechanisms is analysed providing the necessary understanding of the main practical issues affecting the performance of sigma delta modulators The knowledge derived from the first two chapters is presented in the book as an essential part of the systematic top down bottom up synthesis methodology of sigma delta modulators described in Chapter 3 where a time domain behavioural simulator named SIMSIDES is described and applied to the high level design and verification of sigma delta ADCs Chapter 4 moves farther down from system level to the circuit and physical level providing a number of design recommendations and practical recipes to complete the design flow of sigma delta modulators To conclude the book Chapter 5 gives an overview of the state of the art sigma delta ADCs which are exhaustively analysed in order to extract practical design guidelines and to identify the incoming trends design challenges as well as practical solutions proposed by cutting edge designs Offers a complete survey of sigma delta modulator architectures from fundamentals to state of the art topologies considering both switched capacitor and continuous time circuit implementations Gives a systematic analysis and practical design guide of sigma delta modulators from a top down bottom up perspective including mathematical models and analytical procedures behavioural modeling in MATLAB SIMULINK macromodeling and circuit

level implementation in Cadence Design Framework II chip prototyping and experimental characterization Systematic compilation of cutting edge sigma delta modulators Complete description of SIMSIDES a time domain behavioural simulator implemented in MATLAB SIMULINK Plenty of examples case studies and simulation test benches covering the different stages of the design flow of sigma delta modulators A number of electronic resources including SIMSIDES the statistical data used in the state of the art survey as well as many design examples and test benches are hosted on a companion website Essential reading for Researchers and electronics engineering practitioners interested in the design of high performance data converters integrated in nanometer CMOS technologies mixed signal designers Continuous-Time Delta-Sigma Modulators for High-Speed A/D Conversion James A. Cherry, W. Martin Snelgrove, 1999-09-30 Among analog to digital converters the delta sigma modulator has cornered the market on high to very high resolution converters at moderate speeds with typical applications such as digital audio and instrumentation Interest has recently increased in delta sigma circuits built with a continuous time loop filter rather than the more common switched capacitor approach Continuous time delta sigma modulators offer less noisy virtual ground nodes at the input inherent protection against signal aliasing and the potential to use a physical rather than an electrical integrator in the first stage for novel applications like accelerometers and magnetic flux sensors More significantly they relax settling time restrictions so that modulator clock rates can be raised This opens the possibility of wideband 1 MHz or more converters possibly for use in radio applications at an intermediate frequency so that one or more stages of mixing might be done in the digital domain Continuous Time Delta Sigma Modulators for High Speed A D Conversion Theory Practice and Fundamental Performance Limits covers all aspects of continuous time delta sigma modulator design with particular emphasis on design for high clock speeds The authors explain the ideal design of such modulators in terms of the well understood discrete time modulator design problem and provide design examples in Matlab They also cover commonly encountered non idealities in continuous time modulators and how they degrade performance plus a wealth of material on the main problems feedback path delays clock jitter and quantizer metastability in very high speed designs and how to avoid them They also give a concrete design procedure for a real high speed circuit which illustrates the tradeoffs in the selection of key parameters Detailed circuit diagrams simulation results and test results for an integrated continuous time 4 GHz band pass modulator for A D conversion of 1 GHz analog signals are also presented Continuous Time Delta Sigma Modulators for High Speed A D Conversion Theory Practice and Fundamental Performance Limits concludes with some promising modulator architectures and a list of the challenges that remain in this exciting field

**Continuous-Time Sigma-Delta Modulation for A/D Conversion in Radio Receivers** Lucien Breems, Johan Huijsing, 2006-04-18 This text describes the design and theory of continuous time sigma delta modulators for analogue to digital conversion in radio receivers The book's main focus is on dynamic range linearity and power efficiency aspects of sigma delta modulators which are very important requirements for use in battery operated receivers **Robust Sigma**

**Delta Converters** Robert H.M. van Veldhoven, Arthur H.M. van Roermund, 2011-01-30 Sigma Delta converters are a very popular choice for the A/D converter in multi standard mobile and cellular receivers. Key A/D converter specifications are high dynamic range, robustness, scalability, low power and low EMI. Robust Sigma Delta Converters presents a requirement derivation of a Sigma Delta modulator applied in a receiver for cellular and connectivity and shows trade offs between RF and ADC. The book proposes to categorize these requirements in 5 quality indicators which can be used to qualify a system, namely accuracy, robustness, flexibility, efficiency and emission. In the book these quality indicators are used to categorize Sigma Delta converter theory. A few highlights on each of these quality indicators are: Quality indicators provide a means to quantify system quality; Accuracy: introduction of new Sigma Delta Modulator architectures; Robustness: a significant extension on clock jitter theory based on phase and error amplitude error models; Extension of the theory describing aliasing in Sigma Delta converters for different types of DACs in the feedback loop; Flexibility: introduction of a Sigma Delta converter bandwidth scaling theory leading to very flexible Sigma Delta converters; Efficiency: introduction of new Figure of Merits which better reflect performance power trade offs; Emission: analysis of Sigma Delta modulators on emission is not part of the book. The quality indicators also reveal that to exploit nowadays advanced IC technologies things should be done as much as possible: digital up to a limit where system optimization allows reducing system margins. At the end of the book Sigma Delta converter implementations are shown which are digitized on application architecture, circuit and layout level. Robust Sigma Delta Converters is written under the assumption that the reader has some background in receivers and in A/D conversion.

**Sigma-Delta Converters: Practical Design Guide** Jose M. de la Rosa, 2018-08-22 Thoroughly revised and expanded to help readers systematically increase their knowledge and insight about Sigma Delta Modulators. Sigma Delta Modulators (SDMs) have become one of the best choices for the implementation of analog/digital interfaces of electronic systems integrated in CMOS technologies. Compared to other kinds of Analog-to-Digital Converters (ADCs), SDMs cover one of the widest conversion regions of the resolution versus bandwidth plane, being the most efficient solution to digitize signals in an increasingly number of applications which span from high resolution/low bandwidth digital audio sensor interfaces and instrumentation to ultra low power biomedical systems and medium resolution broadband wireless communications. Following the spirit of its first edition, Sigma Delta Converters Practical Design Guide 2nd Edition takes a comprehensive look at SDMs: their diverse types, architectures, circuit techniques, analysis, synthesis methods and CAD tools, as well as their practical design considerations. It compiles and updates the current research reported on the topic and explains the multiple trade offs involved in the whole design flow of Sigma Delta Modulators from specifications to chip implementation and characterization. The book follows a top-down approach in order to provide readers with the necessary understanding about recent advances, trends and challenges in state-of-the-art SDMs. It makes more emphasis on two key points which were not treated so deeply in the first edition: It includes a more detailed explanation of SDMs implemented using Continuous Time CT

circuits going from system level synthesis to practical circuit limitations It provides more practical case studies and applications as well as a deeper description of the synthesis methodologies and CAD tools employed in the design of converters Sigma Delta Converters Practical Design Guide 2nd Edition serves as an excellent textbook for undergraduate and graduate students in electrical engineering as well as design engineers working on SD data converters who are looking for a uniform and self contained reference in this hot topic With this goal in mind and based on the feedback received from readers the contents have been revised and structured to make this new edition a unique monograph written in a didactical pedagogical and intuitive style

**Delta-Sigma Modulators** George I. Bourdopoulos, 2003 This important book deals with the modeling and design of higher order single stage delta sigma modulators It provides an overview of the architectures the quantizer models the design techniques and the implementation issues encountered in the study of the delta sigma modulators A number of applications are discussed with emphasis on use in the design of analog to digital converters and in frequency synthesis The book is education rather than research oriented containing numerical examples and unsolved problems It is aimed at introducing the final year undergraduate the graduate student or the electronic engineer to this field Contents Analog to Digital Conversion ou Modulators OCo Architectures Single Bit Single Stage ou Modulators Modeling and Design Implementation of ou Modulators Practical Limitations of ou Modulators Stabilization and Suppression of Tones for the Higher Order Single Stage ou Modulators Decimation Interpolation and Converters Applications Readership Final year undergraduates graduate students electrical electronic and systems engineers

**Bandpass Sigma Delta Modulators** Jurgen van Engelen, Rudy J. van de Plassche, 1999-10-31 Sigma delta modulation has become a very useful and widely applied technique for high performance Analog to Digital A D conversion of narrow band signals Through the use of oversampling and negative feedback the quantization errors of a coarse quantizer are suppressed in a narrow signal band in the output of the modulator Bandpass sigma delta modulation is well suited for A D conversion of narrow band signals modulated on a carrier as occurs in communication systems such as AM FM receivers and mobile phones Due to the nonlinearity of the quantizer in the feedback loop a sigma delta modulator may exhibit input signal dependent stability properties The same combination of the nonlinearity and the feedback loop complicates the stability analysis In Bandpass Sigma Delta Modulators the describing function method is used to analyze the stability of the sigma delta modulator The linear gain model commonly used for the quantizer fails to predict small signal stability properties and idle patterns accurately In Bandpass Sigma Delta Modulators an improved model for the quantizer is introduced extending the linear gain model with a phase shift Analysis shows that the phase shift of a sampled quantizer is in fact a phase uncertainty Stability analysis of sigma delta modulators using the extended model allows accurate prediction of idle patterns and calculation of small signal stability boundaries for loop filter parameters A simplified rule of thumb is derived and applied to bandpass sigma delta modulators The stability properties have a considerable impact on the design of single loop one bit high order continuous time bandpass sigma delta

modulators The continuous time bandpass loop filter structure should have sufficient degrees of freedom to implement the desired small signal stable sigma delta modulator behavior Bandpass Sigma Delta Modulators will be of interest to practicing engineers and researchers in the areas of mixed signal and analog integrated circuit design Design Techniques for Mash

Continuous-Time Delta-Sigma Modulators Qiyuan Liu,Alexander Edward,Carlos Briseno-Vidrios,Jose

Silva-Martinez,2018-03-27 This book describes a circuit architecture for converting real analog signals into a digital format suitable for digital signal processors This architecture referred to as multi stage noise shaping MASH Continuous Time Sigma Delta Modulators CT M has the potential to provide better digital data quality and achieve better data rate conversion with lower power consumption The authors not only cover MASH continuous time sigma delta modulator fundamentals but also provide a literature review that will allow students professors and professionals to catch up on the latest developments in related technology *Systematic Design of Sigma-Delta Analog-to-Digital Converters* Ovidiu Bajdechi,Johan

Huijsing,2004-04-30 Systematic Design of Sigma Delta Analog to Digital Converters describes the issues related to the sigma delta analog to digital converters ADCs design in a systematic manner from the top level of abstraction represented by the filters defining signal and noise transfer functions STF NTF passing through the architecture level where topology related performance is calculated and simulated and finally down to parameters of circuit elements like resistors capacitors and amplifier transconductances used in individual integrators The systematic approach allows the evaluation of different loop filters order aggressiveness discrete time or continuous time implementation with quantizers varying in resolution Topologies explored range from simple single loops to multiple cascaded loops with complex structures including more feedbacks and feedforwards For differential circuits with switched capacitor integrators for discrete time DT loop filters and active RC for continuous time CT ones the passive integrator components are calculated and the power consumption is estimated based on top level requirements like harmonic distortion and noise budget This unified systematic approach to choosing the best sigma delta ADC implementation for a given design target yields an interesting solution for a high resolution broadband DSL like ADC operated at low oversampling ratio which is detailed down to transistor level schematics The target audience of Systematic Design of Sigma Delta Analog to Digital Converters are engineers designing sigma delta ADCs and or switched capacitor and continuous time filters both beginners and experienced It is also intended for students academics involved in sigma delta and analog CAD research **A Survey on Continuous-time [delta Sigma] Modulators** Xiaoran Gao,2008

Recently delta sigma modulation has become a widely applied technique for high performance analog to digital conversion of narrow band signals Most of the early designs used discrete time structure for good accuracy and good linearity The transfer functions are independent of the clock frequency However high unity gain bandwidths of the opamps are required to satisfy the settling accuracy required in the discrete time designs Continuous time structure can potentially achieve higher clock frequency with less power consumption the anti aliasing filter can also be eliminated due to the anti aliasing property of CT

delta sigma modulators On the other hand CT delta sigma ADC have their own problems such as jitter sensitivity and excess loop delay In this thesis the state of the art of CT delta sigma modulator is reviewed The problems in the design of CT delta sigma ADCs are analyzed and solutions to them are described The theory design and implementations of CT delta sigma modulator will also be reviewed

**How to Improve Performance of Sigma- Delta Analog to Digital Converter** Prateek Verma,2015-04-02 Analog to Digital Converters are widely used in the field of VLSI and are mainly used in the applications like audio instrumentation seismic voice etc which requires higher value of resolution For such applications ADC s can be used based on Nyquist Rate modulators where sampling is done with twice the sampling frequency or Sigma Delta modulators where sampling is done with 15 20 times the sampling frequency ADC based on sigma delta modulators is attractive for VLSI implementation because they are not so sensitive of circuit non idealities and component mismatch However issues such as clock jitter and excess loop delay become great challenges to the designer especially at high sampling frequency Special design should be applied to overcome these problems Sigma Delta modulator can be of different orders like 1st order 2nd order etc and can be continuous time less power consumption or Discrete Time This book demonstrates a Graphical User Interface GUI of 2nd order Sigma Delta modulator which is used to check the non idealities of the circuit Here the model is based on the behavioral modeling of the parameters with the help of Matlab Simulink

**Understanding Delta-Sigma Data Converters** Shanthi Pavan,Richard Schreier,Gabor C. Temes,2017-01-24 This new edition introduces operation and design techniques for Sigma Delta converters in physical and conceptual terms and includes chapters which explore developments in the field over the last decade Includes information on MASH architectures digital to analog converter DAC mismatch and mismatch shaping Investigates new topics including continuous time analog to digital converters ADCs principles and designs circuit design for both continuous time and discrete time ADCs decimation and interpolation filters and incremental ADCs Provides emphasis on practical design issues for industry professionals

*Delta-Sigma Data Converters* Steven R. Norsworthy,Richard Schreier,Gabor C. Temes,1996-10-28 This comprehensive guide offers a detailed treatment of the analysis design simulation and testing of the full range of today s leading delta sigma data converters Written by professionals experienced in all practical aspects of delta sigma modulator design Delta Sigma Data Converters provides comprehensive coverage of low and high order single bit bandpass continuous time multi stage modulators as well as advanced topics including idle channel tones stability decimation and interpolation filter design and simulation

**Design Trade-off of Low Power Continuous-time [Sigma Delta] Modulators for A/D Conversions**

Tongyu Song,2007 The research investigates several critical design issues of continuous time CT Sigma Delta modulators The first is to investigate the sensitivity of CT Sigma Delta modulators to high frequency clock spurs These spurs down convert the high frequency quantization noise degrading the dynamic range of the modulator The second is to study the robustness of continuous time loop filters under large RC product variations Large RC variations in the CMOS process

strongly degrade the performance of continuous time Sigma Delta modulators and reduce the production yield The third is to model the harmonic distortion of one bit continuous time Sigma Delta modulators due to the interaction between the first integrator and the feedback digital to analog converter DAC A closed form expression of the 3<sup>rd</sup> order harmonic distortion is derived and verified Conventional CT Sigma Delta modulators employ all active integrators each integrator needs an active amplifier The research proposes a 5<sup>th</sup> order continuous time Sigma Delta modulator with a hybrid active passive loop filter consisting of only three amplifiers The passive integrators save power and introduce no distortion The active integrators provide gain and minimize internal noise contributions A single bit switched capacitor DAC is employed as the main feedback DAC for high clock jitter immunity An additional current steering DAC stabilizes the loop with the advantage of simplicity To verify the proposed techniques a prototype continuous time Sigma Delta modulator with 2 MHz signal bandwidth is designed in a 0.25  $\mu$ m CMOS technology targeting for GPS or WCDMA applications The experimental results show that the prototype modulator achieves 68 dB dynamic range over 2 MHz bandwidth with a 150 MHz clock consuming 1.8 mA from a 1.5 V supply

**Design of Multi-Bit Delta-Sigma A/D Converters** Yves Geerts, Michiel Steyaert, Willy M. C. Sansen, 2002-05-31

This book discusses both architecture and circuit design aspects of Delta Sigma A/D converters with a special focus on multi-bit implementations The emphasis is on high speed high resolution converters in CMOS for ADSL applications although the material can also be applied for other specification goals and technologies

**Power Efficient Continuous-time**

**Delta-sigma Modulator Architectures for Wideband Analog to Digital Conversion** Mohammad Ranjbar, 2012 This work presents novel continuous time delta sigma modulator architectures with low power consumption and improved signal transfer functions which are suitable for wideband A/D conversion in wireless applications e.g. 3G and 4G receivers The research has explored two routes for improving the overall performance of continuous time delta sigma modulator The first part of this work proposes the use of the power efficient Successive Approximations SAR architecture instead of the conventional Flash ADC as the internal quantizer of the delta sigma modulator The SAR intrinsic latency has been addressed by means of a faster clock for the quantizer as well as full period delay compensation The use of SAR quantizer allows for increasing the resolution while reducing the total power consumption and complexity A higher resolution quantizer made feasible by the SAR would allow implementing more aggressive noise shaping to facilitate wideband delta sigma A/D conversion at lower oversampling rates As proof of concept a first order CT delta sigma modulator with a 5-bit SAR quantizer is designed and implemented in a 130 nm CMOS process which achieves 62 dB dynamic range over 1.92 MHz signal bandwidth meeting the requirements of the WCDMA standard The prototype modulator draws 3.1 mW from a single 1.2 V supply and occupies 0.36 mm<sup>2</sup> of die area The second part of this research addresses the issue of out of band peaking in the signal transfer function STF of the widely used feedforward structure The STF peaking is harmful to the performance of the modulator as it allows an interferer to saturate the quantizer and result in severe harmonic distortion and instability As a

remedy to this problem a general low pass and peaking free STF design methodology has been proposed which allows for implementing an all pole filter in the input signal path for any given NTF Based on the proposed method the STF peaking of any feedforward modulator can be eliminated using extra feed in paths to all the integrator inputs A major drawback of the conventional feedforward topology having low pass STF is the large sensitivity of the STF to the coefficients In particular component mismatch due to random errors in the relative values of individual resistors or capacitors can significantly degrade the anti aliasing of the CT modulator and give rise to the unwanted STF peaking To solve this problem two new architectures namely dual feedback and dual feed in are proposed which allow us to synthesize a low pass STF with a smaller number of coefficients than the feedforward structure The dual feedback structure which shows significantly lower sensitivity to coefficient mismatch is extensively analyzed and simulated Also for proof of concept a third order modulator is implemented in a 130 nm CMOS process which achieves 76 dB dynamic range over 5 MHz signal bandwidth meeting for example the requirements of a DVB H receiver standard In addition the modulator shows 77 dB anti aliasing and less than 0.1 dB worst case STF peaking The measured power consumption of the modulator is 6 mW from a single 1.2 V and the die area is 0.56 mm<sup>2</sup>

**Delta-Sigma A/D-Converters** Richard Gaggli, 2012-12-17 The emphasis of this book is on practical design aspects for broadband A/D converters for communication systems The embedded designs are employed for transceivers in the field of ADSL solutions and WLAN applications An area and power efficient realization of a converter is mandatory to remain competitive in the market The right choice for the converter topology and architecture needs to be done very carefully to result in a competitive FOM The book begins with a brief overview of basic concepts about ADSL and WLAN to understand the ADC requirements At architectural level issues on different modulator topologies are discussed employing the provided technology node The design issues are pointed out in detail for modern digital CMOS technologies beginning with 180nm followed by 130nm and going down to 65nm feature size Beside practical aspects challenges to mixed signal design level are addressed to optimize the converters in terms of consumed chip area power consumption and design for high yield in volume production Thus careful considerations on circuit and architectural level are performed by introducing a dynamic biasing technique a feed forward approach and a resolution in time instead of amplitude resolution

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